

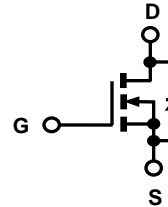


PMG20N170G N-Channel Enhancement Mode MOSFET

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

Product Summary			
I_D	$T_A=25^\circ\text{C}$	20A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	600V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.17 Ω	Typ
Q_g	$V_{DS}=480\text{V}$	62nC	Typ



T0263

Standard Metal
Heatsink

1=Gate, 2&4=Drain,
3=Source.

Maximum ratings^b, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_c=25^\circ\text{C}$	20	A
Pulsed drain current	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	62	A
Avalanche energy, single pulse	E_{AS}	$I_D=10\text{A}$	520	mJ
Avalanche current, repetitive	I_{AR}	limited by T_j max	20	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=480\text{V}$, $I_D=20\text{A}$, $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	V_{GS}	static	± 20	V
		AC ($f > 1\text{Hz}$)	± 30	
Power dissipation	P_{tot}	$T_c=25^\circ\text{C}$	208	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	$^\circ\text{C}$
Mounting torque		M 3 & 3.5 screws	60	Ncm

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Thermal resistance, junction-case ^a	R_{thJC}		-	-	0.7	°C/W
Thermal resistance, junction-ambient ^a	R_{thJA}	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics ^b, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	600	640	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$	-	0.1	1	μA
		$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=150^\circ\text{C}$	-	-	100	
Gate source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=25^\circ\text{C}$	-	0.17	0.19	Ω
		$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=150^\circ\text{C}$	-	0.52	-	
Gate resistance	R_G	$f=1\text{ MHz}, \text{open drain}$	-	4.3	-	Ω

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	2020	-	pF
Output capacitance	C_{oss}		-	980	-	
Reverse transfer capacitance	C_{rss}		-	9	-	
Transconductance	g_{fs}	$V_{DS}>2 * I_D * R_{DS}, I_D=10\text{A}$	-	19	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=20\text{A}, R_G=4\Omega \text{ (External)}$	-	39	-	ns
Rise time	t_r		-	3.5	-	
Turn-off delay time	$t_{d(off)}$		-	55	-	
Fall time	t_f		-	7	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

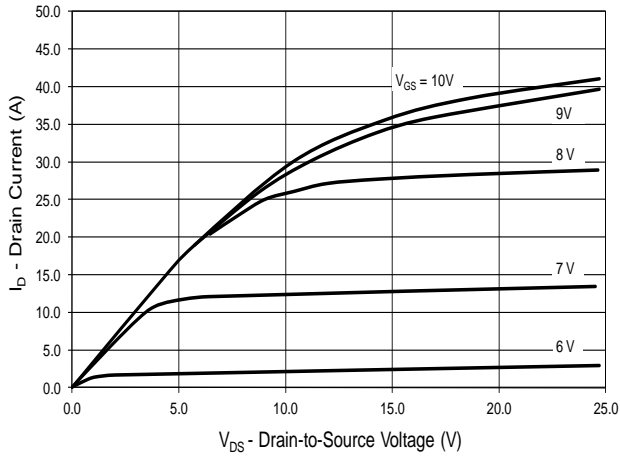
Gate charge characteristics

Gate to source charge	Q_{gs}	$V_{DS}=480\text{ V}, I_D=20\text{ A},$ $V_{GS}=10\text{ V}$	-	13	-	nC
Gate to drain charge	Q_{gd}		-	23	-	
Gate charge total	Q_g		-	62	-	
Gate plateau voltage	V_{plateau}		-	5.8	-	V

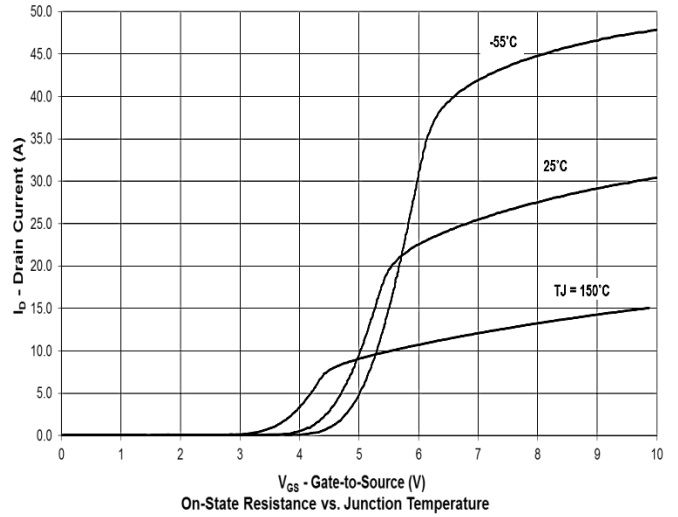
Reverse Diode

Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	$V_{RR}=480\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	407	-	ns
Reverse recovery charge	Q_{rr}		-	6.7	-	μC
Peak reverse recovery current	I_{rm}		-	32	-	A

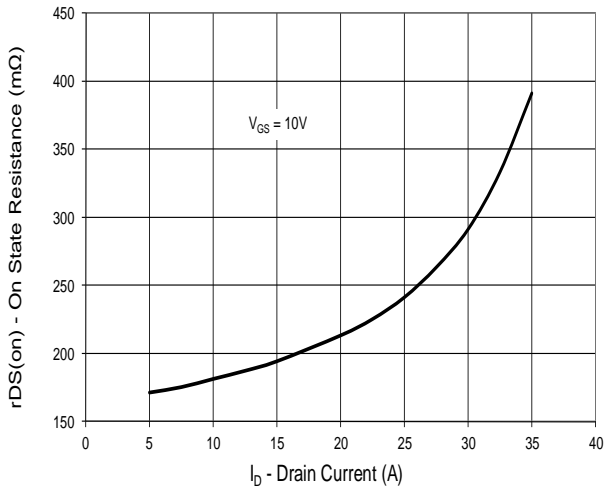
Output Characteristics



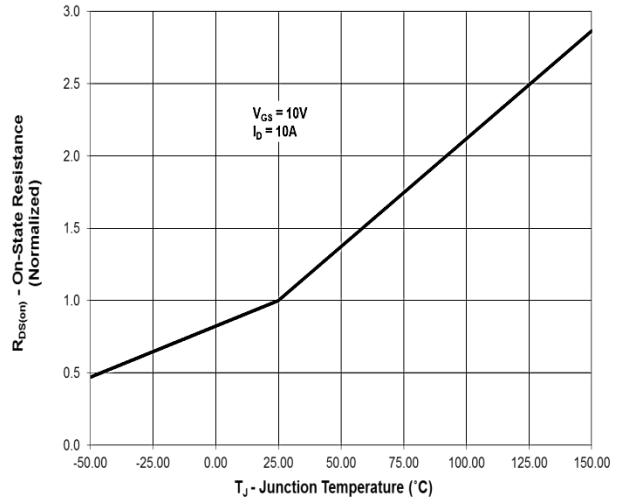
Transfer Characteristics



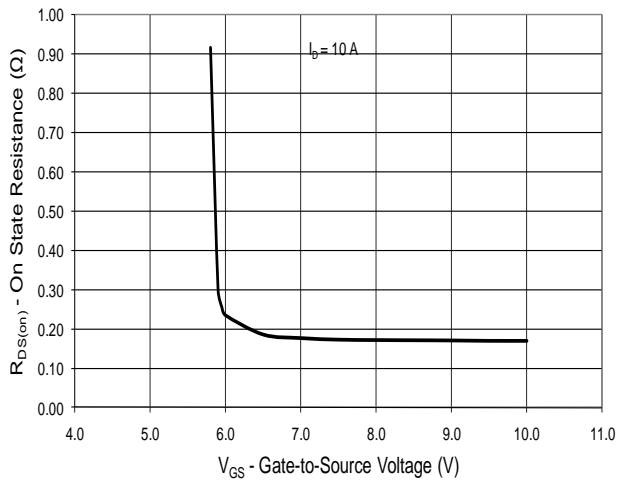
On State Resistance vs. Drain Current



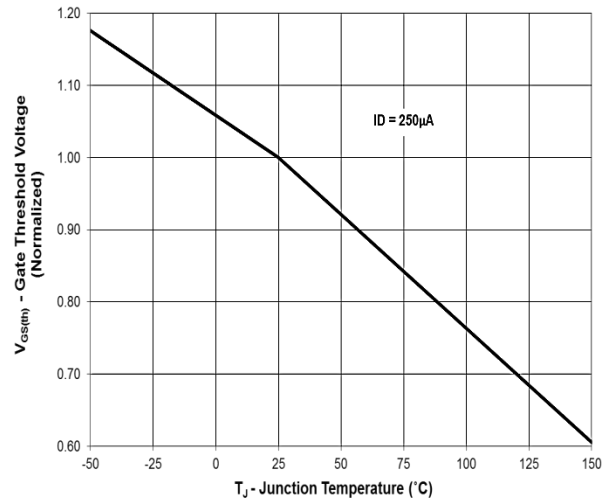
On-State Resistance vs. Junction Temperature



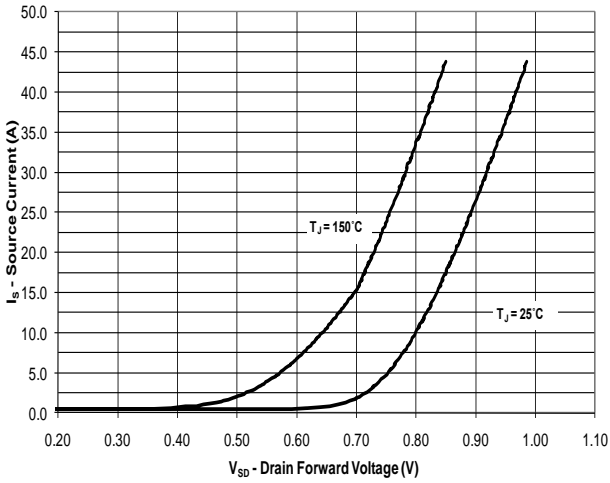
On-Resistance vs. Gate-to-Source Voltage



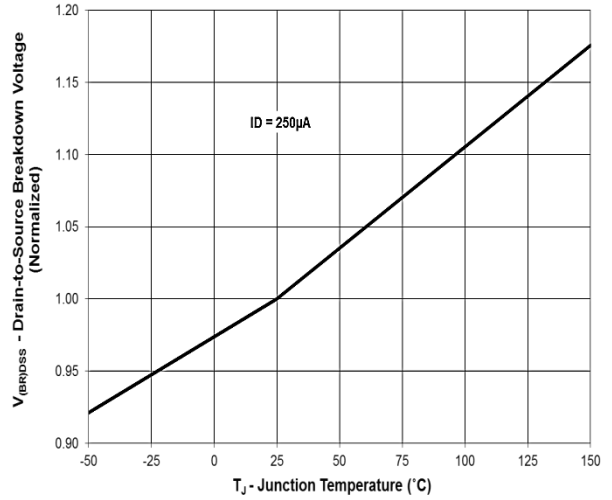
Gate Threshold Voltage vs. Junction Temperature



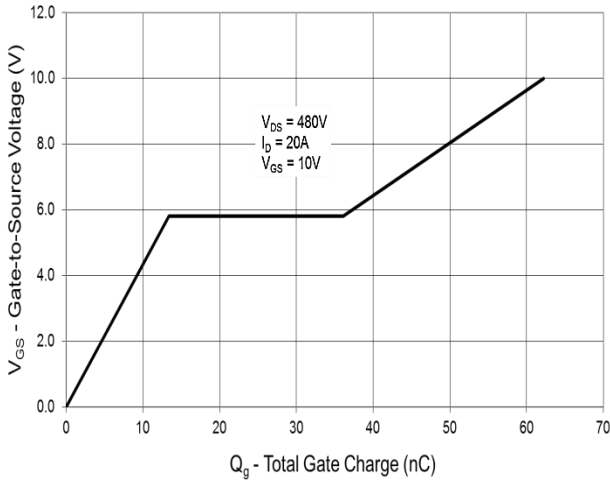
Source-Drain Forward Voltage



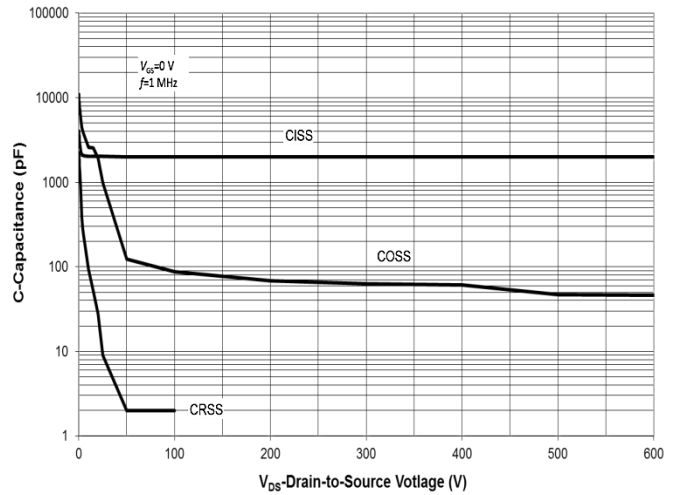
Drain-to-Source Breakdown Voltage vs. Junction Temperature



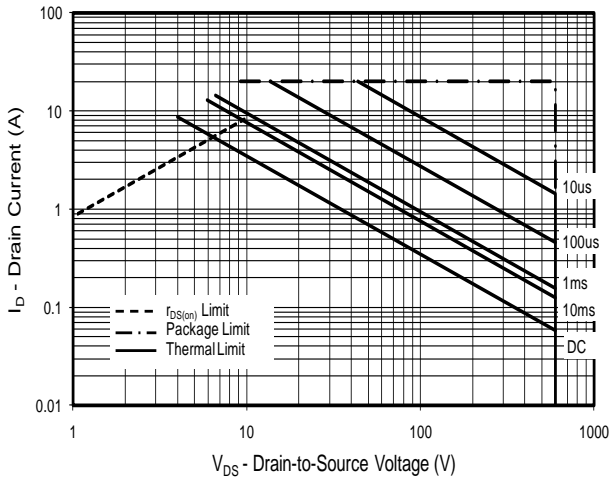
Gate Charge



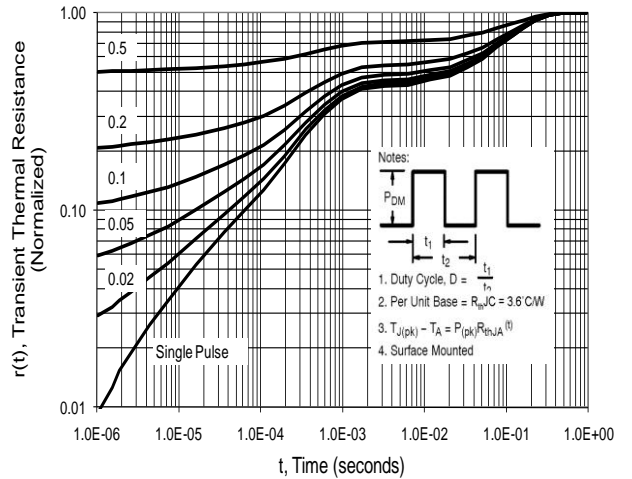
Capacitance

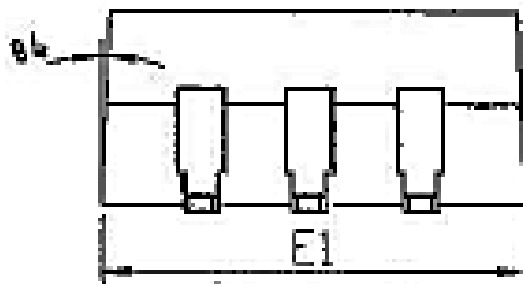
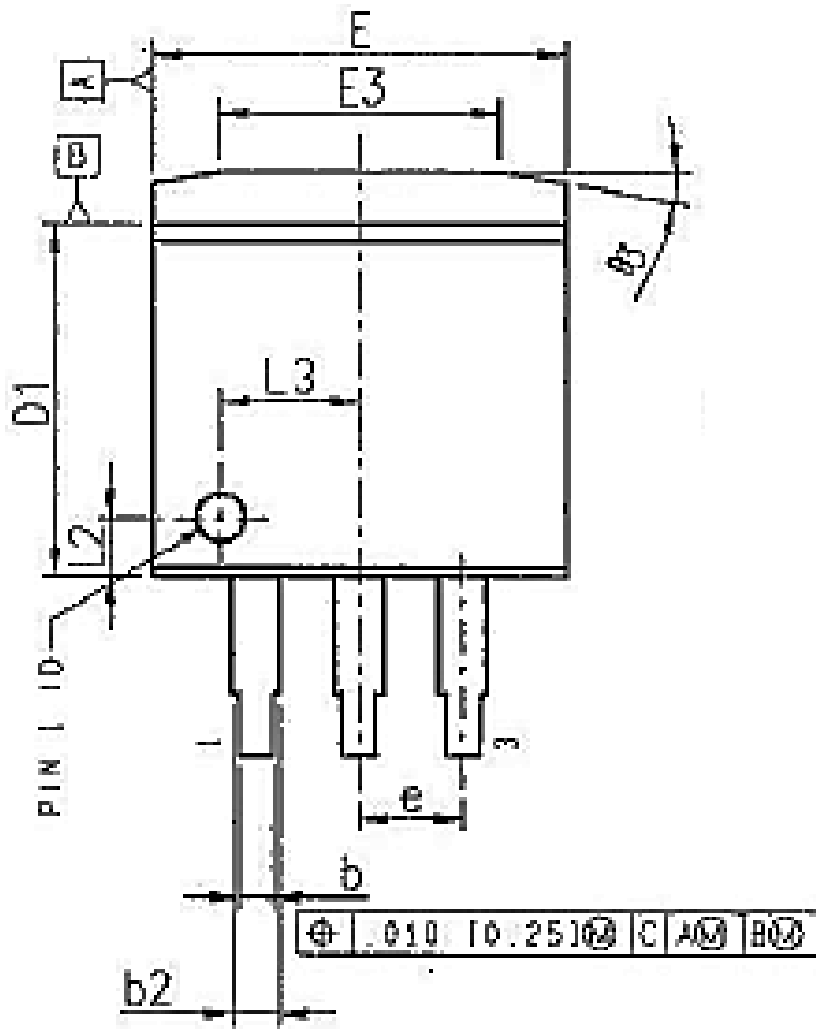


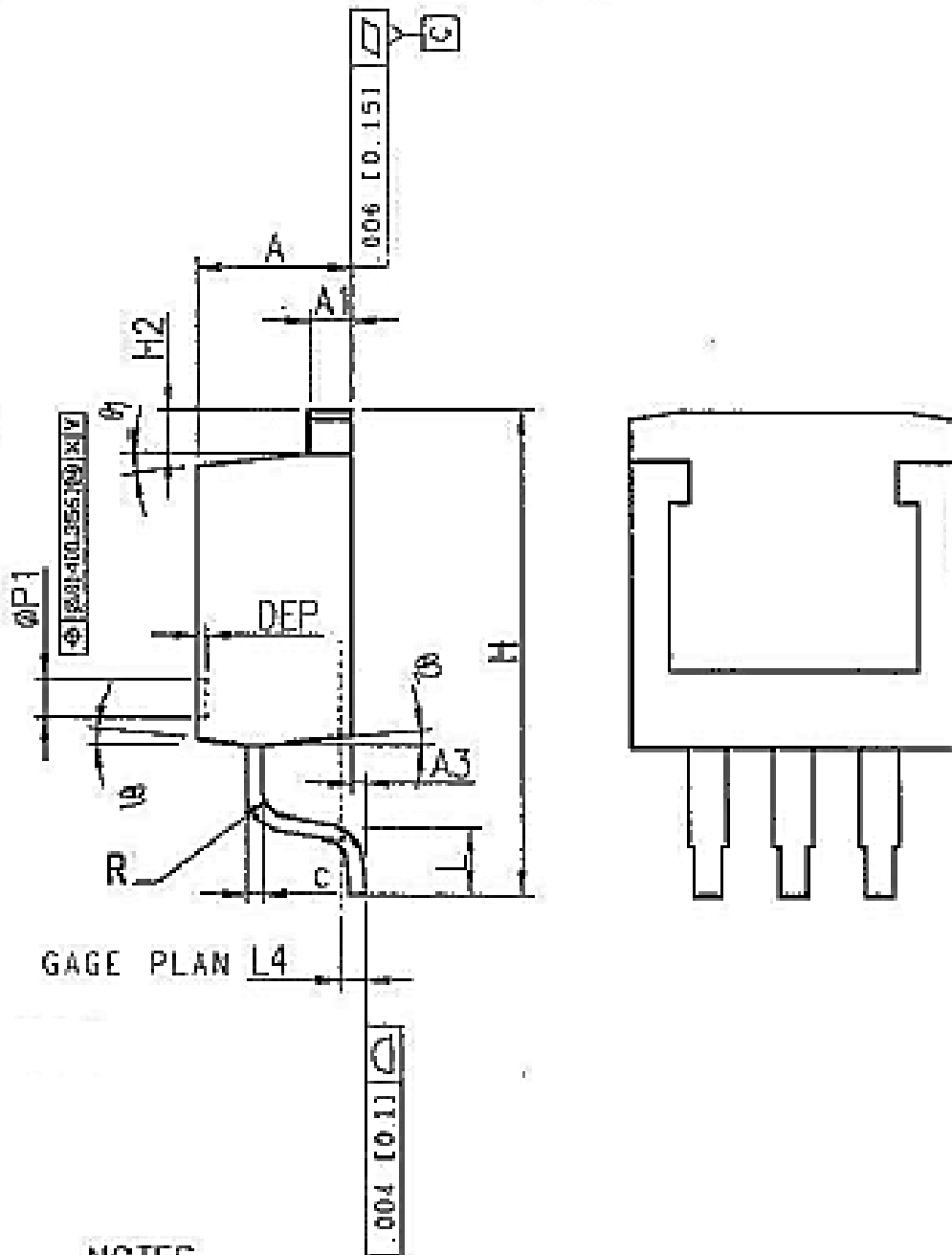
Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case







NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-263, DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

COMMON DIMENSIONS						
SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.45	4.57	4.64	0.175	0.180	0.183
A1	1.22	1.27	1.32	0.048	0.050	0.052
A3	0	-	0.15	0.000	-	0.006
b	0.71	-	0.97	0.028	-	0.038
b2	1.22	-	1.40	0.048	-	0.055
c	0.38	-	0.76	0.015	-	0.030
D1	8.38	8.70	8.89	0.330	0.343	0.350
E	9.91	10.16	10.39	0.390	0.400	0.410
E1	10.03	10.16	10.54	0.395	0.400	0.415
E3	6.61	6.86	7.11	0.260	0.270	0.280
e	2.54BSC			0.100BSC		
H	-	-	14.35	-	-	0.565
H2	-	-	1.27	-	-	0.050
L	-	1.98	-	-	0.078	-
L2	1.47REF			0.058REF		
L3	3.40REF			0.134REF		
L4	-	0.76	-	-	0.30	-
ØP1	1.07	1.20	1.32	0.042	0.047	0.052
R	-	-	0.76	-	-	0.030
θ1	-	7°	-	-	7°	-
θ2	-	3°	-	-	3°	-
θ3	7°	10°	13°	7°	10°	13°
θ4	-	3°	-	-	-	-
DEP	0.10	0.18	0.25	0.004	0.007	0.010