

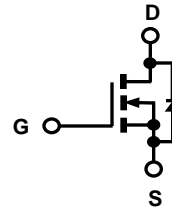


# PMG10N65F N-Channel Enhancement Mode MOSFET

## Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High  $dv/dt$  capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

Product Summary			
$I_D$	$T_A=25^\circ\text{C}$	9.5A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	650V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.35	Typ
$Q_g$	$V_{DS}=480\text{V}$	41nC	Typ



**T0220 Full-PAK  
Isolated (T0-220)**  
1=Gate, 2=Drain,  
3=Source

**Maximum ratings**<sup>b</sup>, at  $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_c=25^\circ\text{C}$	9.5	A
Pulsed drain current	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	28.5	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=8.3\text{A}$	340	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_j$ max	5	A
MOSFET $dv/dt$ ruggedness	$dv/dt$	$V_{DS}=480\text{V}$ , $I_D=9.5\text{A}$ , $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	$V_{GS}$	static	$\pm 20$	V
		AC ( $f > 1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	35	W
Operating and storage temperature	$T_j, T_{stg}$		-55 to +150	$^\circ\text{C}$
Mounting torque		M 2.5 screws	50	Ncm

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Thermal characteristics

Thermal resistance, junction-case <sup>a</sup>	$R_{thJC}$		-	-	3.5	°C/W
Thermal resistance, junction-ambient <sup>a</sup>	$R_{thJA}$	leaded	-	-	80	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

### Electrical characteristics <sup>b</sup>, at $T_j=25^{\circ}\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	650	675	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=150^{\circ}\text{C}$	-	-	100	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=4.75\text{A}, T_j=25^{\circ}\text{C}$	-	0.35	0.38	$\Omega$
		$V_{GS}=10\text{V}, I_D=4.75\text{A}, T_j=150^{\circ}\text{C}$	-	0.63	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	5	-	$\Omega$

#### Dynamic characteristics

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	1250	-	$\mu\text{F}$
Output capacitance	$C_{oss}$		-	600	-	
Reverse transfer capacitance	$C_{rss}$		-	5	-	
Transconductance	$g_{fs}$	$V_{DS}>2 \cdot I_D \cdot R_{DS}, I_D=4.75\text{A}$	-	12	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=9.5\text{A}, R_G=4\Omega$ (External)	-	6	-	ns
Rise time	$t_r$		-	3.5	-	
Turn-off delay time	$t_{d(off)}$		-	54	-	
Fall time	$t_f$		-	7	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

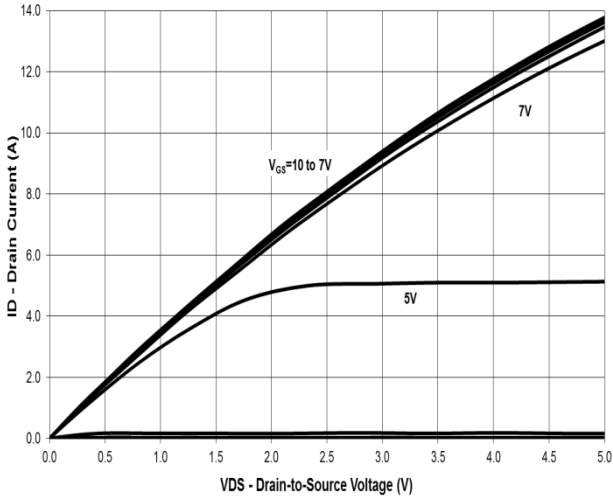
### Gate charge characteristics

Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=9.5\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	7.1	-	nC
Gate to drain charge	$Q_{gd}$		-	14.5	-	
Gate charge total	$Q_g$		-	41	-	
Gate plateau voltage	$V_{\text{plateau}}$		-	5.2	-	V

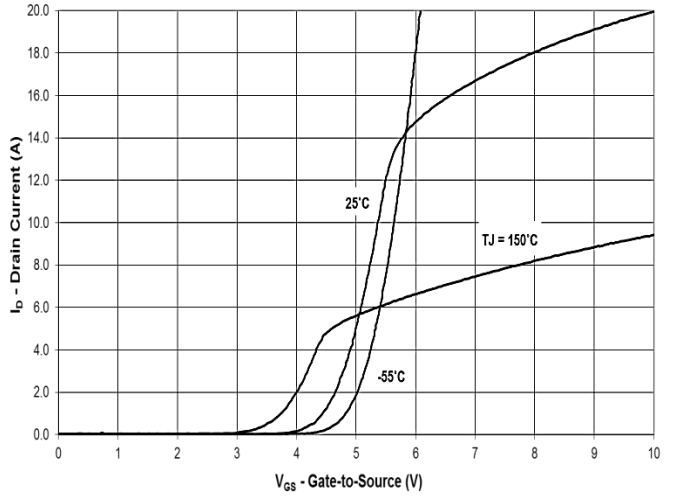
### Reverse Diode

Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=300\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	332	-	ns
Reverse recovery charge	$Q_{rr}$		-	4.4	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rm}$		-	25.6	-	A

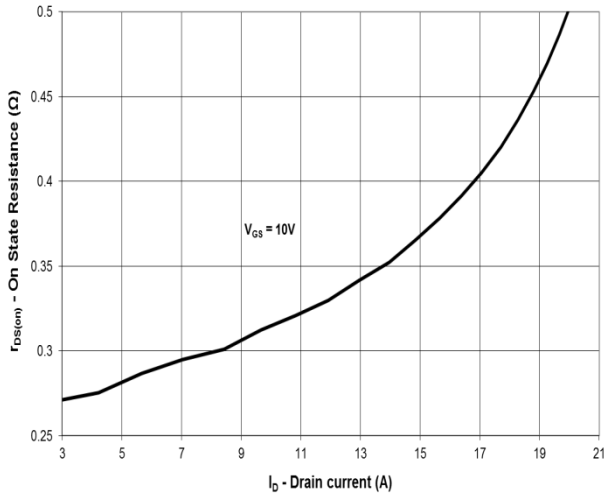
Output Characteristics



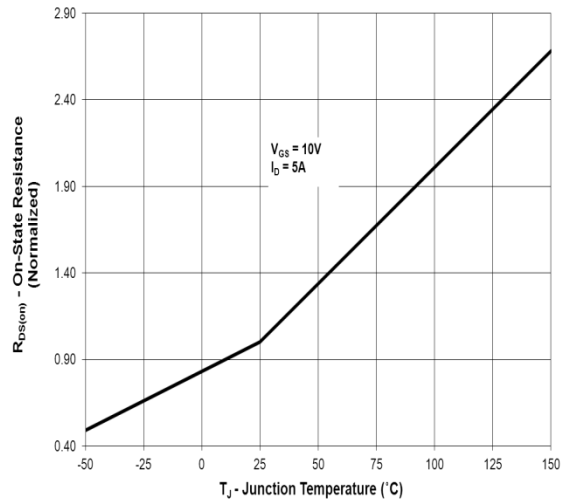
Transfer Characteristics



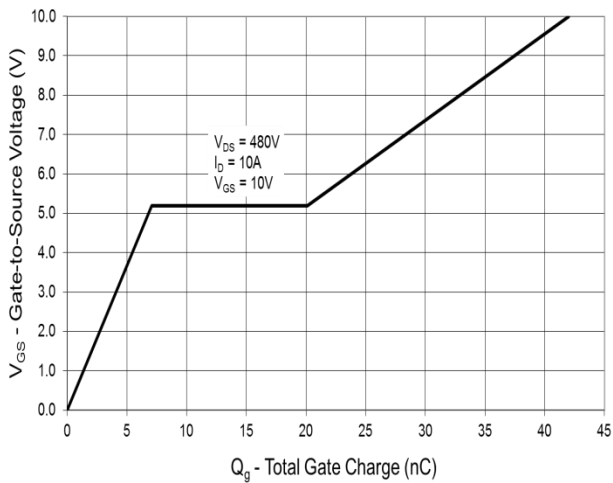
On Resistance vs. Drain Current



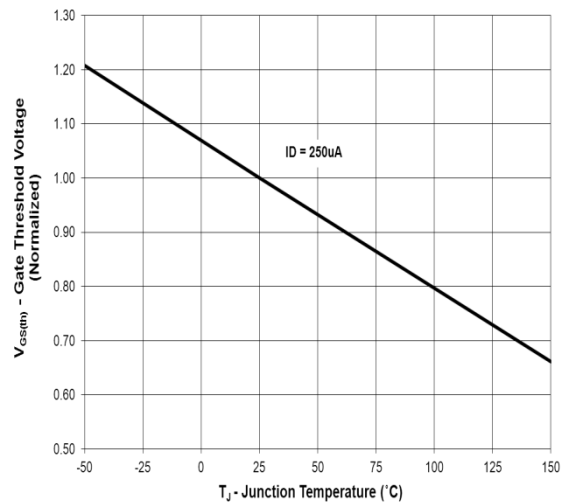
On-State Resistance vs. Junction Temperature



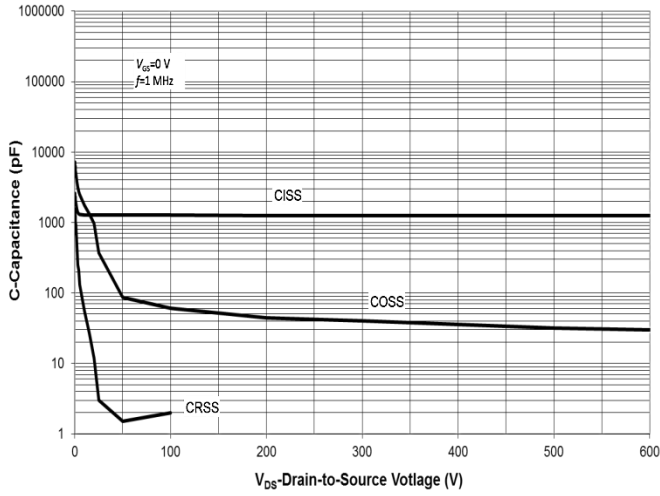
Gate Charge



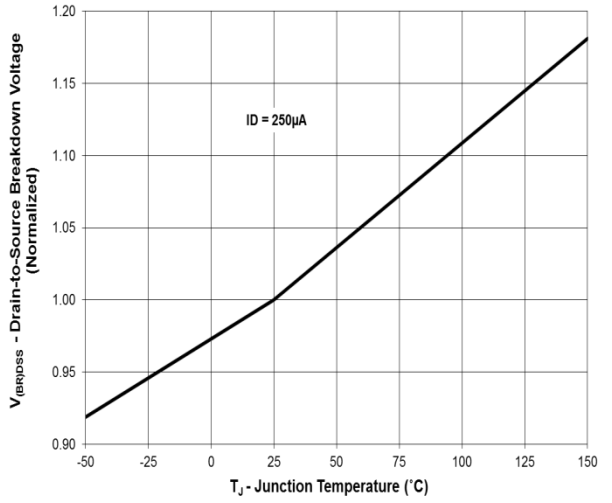
Gate Threshold Voltage vs. Junction Temperature



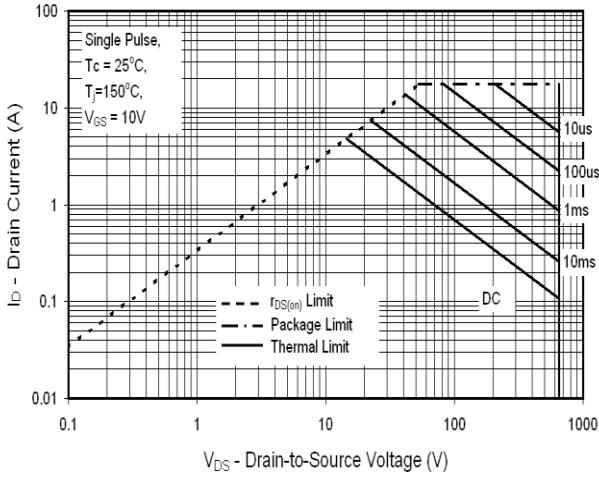
Capacitance



Drain-to-Source Breakdown Voltage vs. Junction Temperature



Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case

